

### Sol.1 (a)

Logical steps:

1. To multiply 2 No's we store 2 data bytes in register D&C(N<sub>1</sub>&N<sub>2</sub>)
2. To initialize BC pair place 00 in B register and N<sub>2</sub> in register C
3. Initialize HL pair for result place 00 in H and 00 in L
4. Perform the multiplication by adding N<sub>2</sub> to result N<sub>1</sub> times use N<sub>1</sub> as counter

MVI D,N<sub>1</sub> : Load 1<sup>st</sup> Number

MVI C,N<sub>2</sub> : Load 2<sup>nd</sup> Number

MVI B,00H : Clear B

LXI H,0000H : Clear HL

UP: DAD B : Add register BC to HL

DCR D : Decrement D

JNZ UP : Go to UP if Z is not zero

HLT

### Sol.1 (b)

$$\begin{aligned} \text{Average time} &= 9 + \frac{0.5}{7200} \times 60 + \frac{0.5}{4 \times 10^3} \\ &= 9 + \frac{30}{7200} + 0.125 = 9 + 4.16 + 0.125 \end{aligned}$$

$$T_{\text{avg.}} = 13.285 \text{ msec}$$

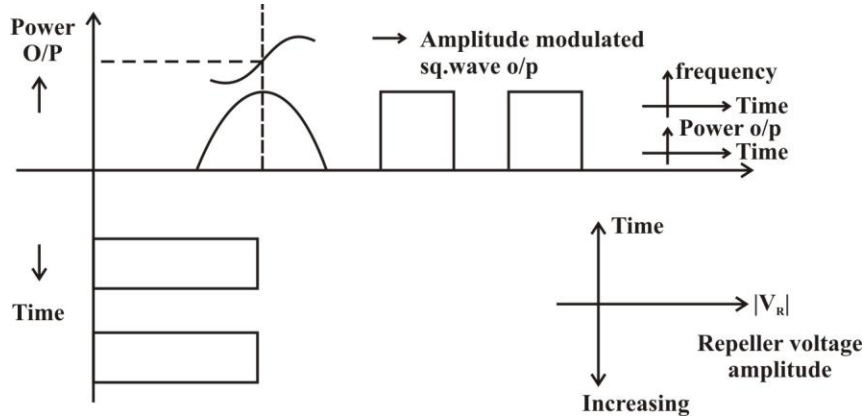
### Sol.1 (c)

Here P-N junction diode is reverse biased beyond the breakdown region so that current density is larger which decreases electric field in space charge region and increases the carrier transit time frequency of operation gets less than 10 GHz but efficiency gets less than 10 GHz but efficiency gets increased due to low power dissipation.

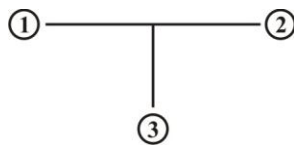
Inside a coaxial resonator TRPATT diode is mounted at a point where maximum RF voltage swing is obtained when combined DC bias and RF voltage exceeds break down voltage avalanche occurs and plasma of electrons and holes are generated which gets trapped. when external circuit current flows voltage rises and trapped plasma gets released producing current pulse across drift space. Here total transit time is sum of drift time and delay introduced by released of trapped plasma. Due to longer transit time operating frequency is limited to 10 GHz because current pulse is associated with low voltage power dissipation is low resulting in higher efficiency.

**Sol.1 (d)**

Simple type of modulation commonly occur in Microwave is sq.wave amplitude produced by modulating reflector voltage. Another modulation used is amplitude modulation of reflector voltage about centre of the mode giving thereby nearly linear frequency modulation character with accompanying amplitude modulation to a degree dependent upon execution of modulated voltage.



**Sol.2 (a)** For a lossless reciprocal 3-port junction, it is impossible to achieve matching at all three ports.



Let all 3 ports are matched:  $\therefore s_{11} = s_{22} = s_{33} = 0$

$$[s] = \begin{bmatrix} 0 & s_{12} & s_{13} \\ s_{21} & 0 & s_{23} \\ s_{31} & s_{32} & 0 \end{bmatrix}$$

By reciprocal property:

$$s_{12} = s_{21}, s_{13} = s_{31}, s_{23} = s_{32}$$

$$[s] = \begin{bmatrix} 0 & s_{12} & s_{13} \\ s_{12} & 0 & s_{23} \\ s_{13} & s_{23} & 0 \end{bmatrix} \quad [s]^* = \begin{bmatrix} 0 & s_{12}^* & s_{13}^* \\ s_{12}^* & 0 & s_{23}^* \\ s_{13}^* & s_{23}^* & 0 \end{bmatrix}$$

By unitary property; we know  $[s][s]^* = I$

$$\begin{bmatrix} 0 & s_{12} & s_{13} \\ s_{12} & 0 & s_{23} \\ s_{13} & s_{23} & 0 \end{bmatrix} \begin{bmatrix} 0 & s_{12}^* & s_{13}^* \\ s_{12}^* & 0 & s_{23}^* \\ s_{13}^* & s_{23}^* & 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$R_1 C_1 = 1 \longrightarrow |s_{12}|^2 + |s_{13}|^2 = 1 \quad \text{--- (i)}$$

$$R_2 C_2 = 1 \longrightarrow |s_{12}|^2 + |s_{23}|^2 = 1 \quad \text{--- (ii)}$$

$$R_3 C_3 = 1 \longrightarrow |s_{13}|^2 + |s_{23}|^2 = 1 \quad \text{--- (iii)}$$

By (i) and (ii):  $|s_{13}| = |s_{23}|$

(ii) and (iii):  $|s_{12}| = |s_{13}|$

$\therefore |s_{12}| = |s_{13}| = |s_{23}|$  — (iv)

$R_1 C_2 = 0 \longrightarrow [s_{13}] [s_{23}^*] = 0$

Either  $s_{13} = 0$  or  $s_{23} = 0$  — (v)

But  $s_{13} = s_{23}$  So it is not possible hence all three ports can't be perfectly matched.

**Sol.2 (b)** Insertion loss = 1dB =  $-20 \log |s_{21}|$   $\therefore s_{21} = 0.83$

So on similar line  $s_{32} = 0.83, s_{13} = 0.83$

Isolation loss = 30dB =  $-20 \log |s_{31}|$

$|s_{31}| = |s_{23}| = |s_{12}| = 0.032$

$K = 0.2 \quad |s_{11}| = |s_{22}| = |s_{33}| = 0.2$

$$S = \begin{bmatrix} 0.2 & 0.032 & 0.83 \\ 0.83 & 0.2 & 0.032 \\ 0.032 & 0.83 & 0.2 \end{bmatrix}$$

**Sol. 2(c)**  $S = \begin{bmatrix} 0 & -s_{12} \\ s_{21} & 0 \end{bmatrix} \rightarrow$  for Gyrator

$S = \begin{bmatrix} 0 & 0 \\ s_{21} & 0 \end{bmatrix} \rightarrow$  for Isolator

**Sol. 3(a)** Electrons just leaving the cathode is:  $v_0 = 0.593 \times 10^6 \sqrt{10^3} = 1.88 \times 10^7$  m/s

Gap Transit angle is:  $\theta_g = \frac{wd}{v_0} = 2 \times \pi \times 3 \times 10^9 \times \frac{10^{-3}}{1.88 \times 10^7} = 1$  rad

Beam coupling coefficient is:  $\beta = \frac{\sin(\theta_g / 2)}{\theta_g / 2} = 0.952$

DC transit angle between the cavities  $\theta_0 = \frac{wL}{v_0} = \frac{2 \times \pi \times 3 \times 10^9 \times 4 \times 10^{-2}}{1.88 \times 10^7} = 40$  rad

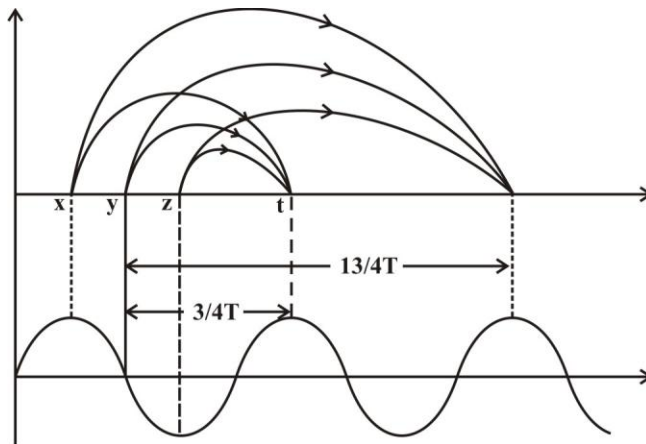
For maximum output voltage

$X = \frac{\alpha \beta \theta_0}{2} = \frac{V_1}{2 \times 1000} \times 0.952 \times 40 = 1.841$

$V_{1\max} = 96.5V$

Value of bunching parameter  $X = 1.841$

Sol.3 (b)



Sol.3(c)  $N = 50 \text{ turns/cm}$   $d = 2 \text{ mm}$

$$v_p = \frac{pc}{\pi d} \quad p \rightarrow \text{pitch} \quad p = \frac{10^{-2}}{50}$$

$$\therefore v_p = \frac{10^{-2} \times 3 \times 10^8}{50 \times 3.14 \times 2 \times 10^{-3}} = 9.5 \times 10^6 \text{ m/sec}$$

Sol.4 (a) InP diode has a large peak to valley current ratio because an electron transfer proceed rapidly as the field increases. This situation occurs because there is weak coupling between lower valley and upper valley in InP than GaAs. The Middle valley energy level provides additional energy loss mechanism required to avoid break down caused by high energy acquired by lower valley electrons from weak coupling.

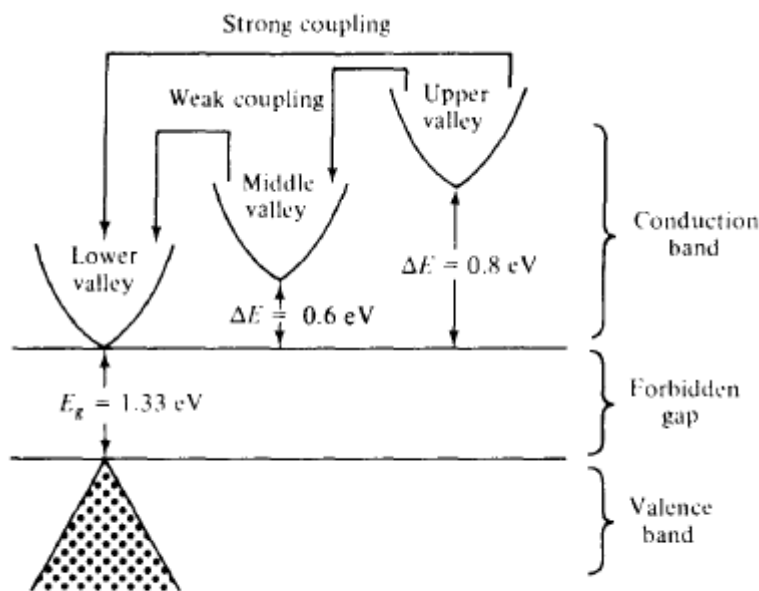
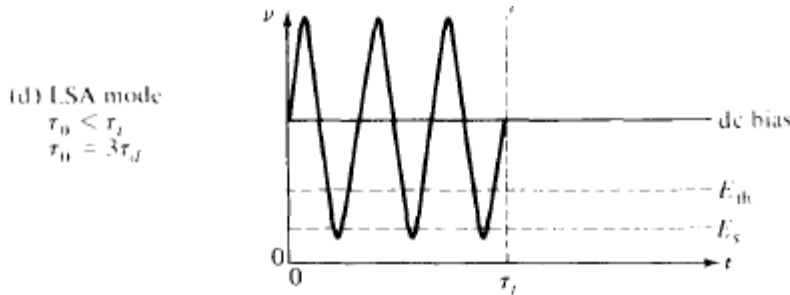


Figure 7-5-1 Three-valley-model energy level for InP diode.

**Sol.4 (b)** when the frequency is high domain don't have sufficient time to form while field is above threshold. As result most of the domains are maintained in negative conductance state during a large fraction of the voltage cycle. Any accumulation of electrons near the cathode has time to collapse while the signal is below threshold. Thus LSA mode is the simple mode of operation and it consists of a uniformly doped semiconductor without any internal space charges. In this case internal field will be uniform and Proportional to the applied voltage. The current in device is then proportional to drift velocity at this field level. The efficiency of the LSA mode can be 20%

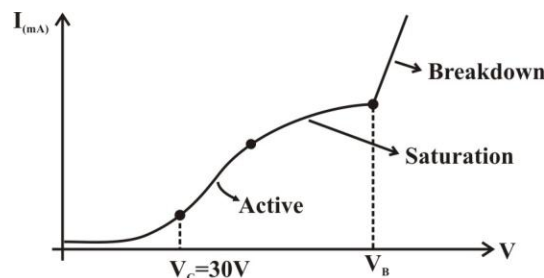


**Sol.4 (c)**

Frequency of operation is:  $f = \frac{v_d}{2L} = \frac{4 \times 10^5}{2 \times 12 \times 10^{-6}} = 0.16 \times 10^{11} = 16 \text{GHz}$

Maximum CW output power =  $0.1 \times 100 \times 100 \times 10^{-3} = 1 \text{W}$

**Sol.4 (d)**



**Sol.5(a)**

LXI H, 4000H	H&L Load with 4000
MOV A,M	Contents of memory copied
ADI 00H	Add Immediate zero
JPE:Odd	
MVI M,DDH	If Parity is odd then store in 00
Odd: MVI M,EEH	If Parity is even then store to 4000
HLT	

Sol. 5(b)

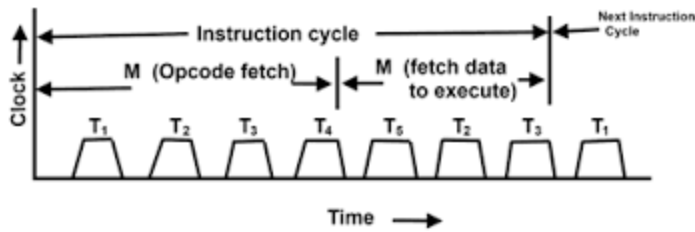


Figure 5: A Typical Instruction Cycle

Sol. 5(c)

When an interrupt is acknowledged by Microprocessor then this reset the interrupt and enable FF and Disable all interrupts. If software instruction EI is inserted then it sets the Interrupt Flags.

**Sol. 6(a)**

Details of Interrupts in 8085 is as follows:

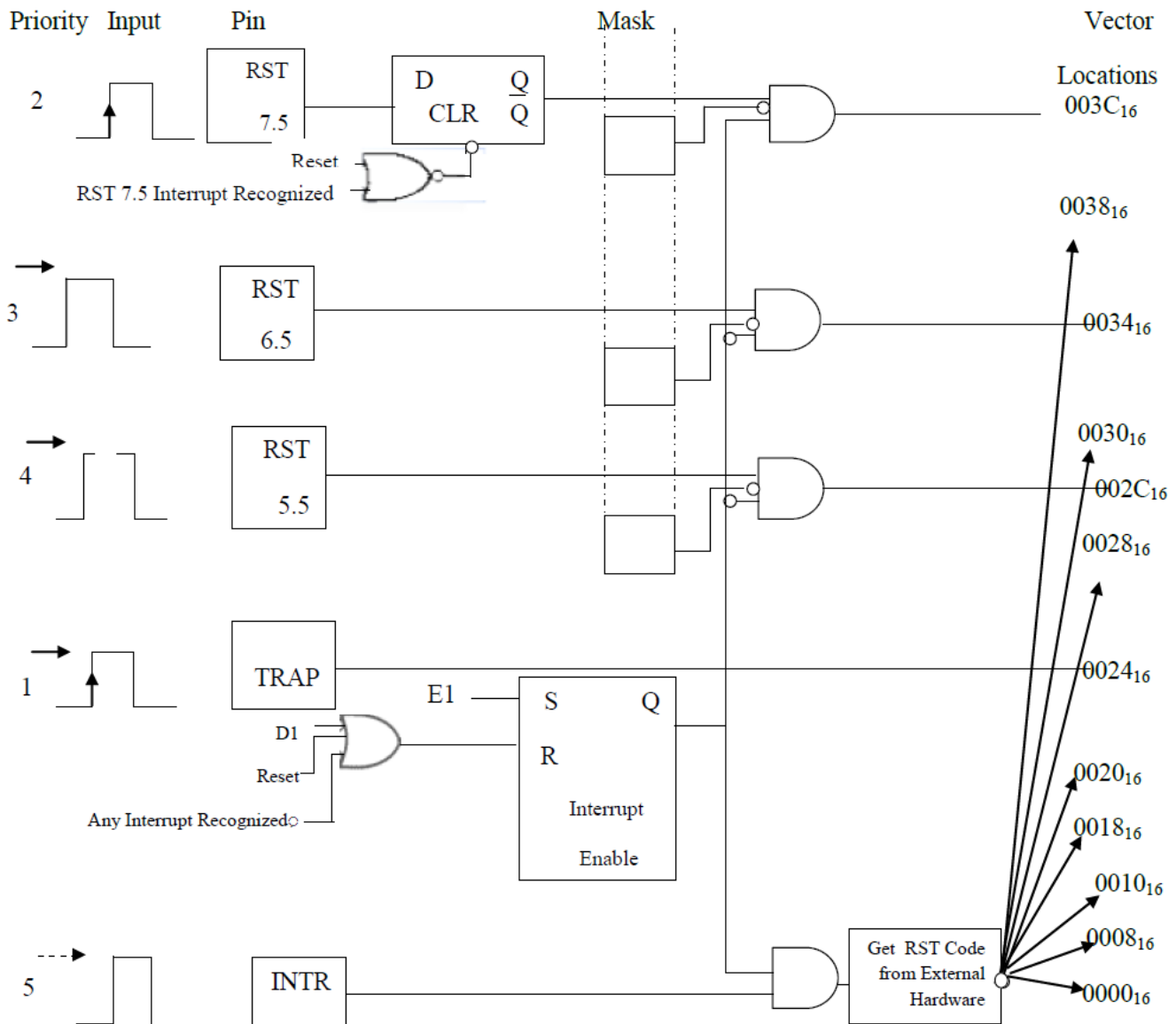


Figure (12.1) The 8085 Interrupts and Vector Locations.

**Sol. 6(b)**

Let crystal frequency of 8085 is 5 MHz. So operating frequency of 8085 is 2.5 MHz

Here Delay is of 0.4 sec so Number of counts= 160000

LXI B, Count: 16 bit register

BACK: DCX B

MOV A,C

ORA B

JNZ BACK

HLT

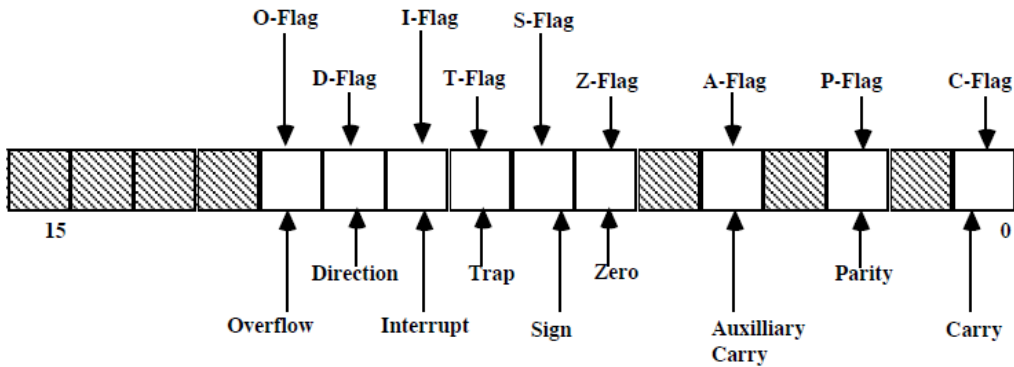


**Sol. 6(c)**

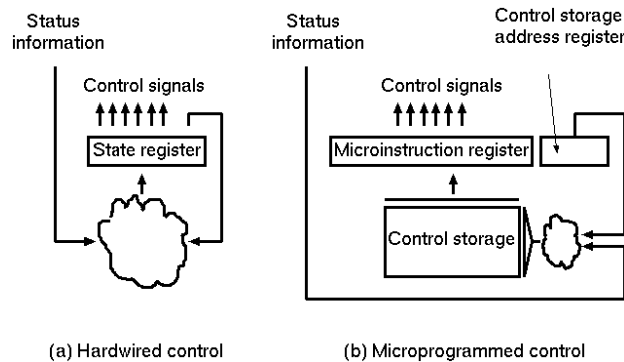
Nine individual bits of status registers are used as control flags (3) and status flags (6). The remaining (6) of them are not used. A flag can take on the values 0 and 1. We say a flag is set if it has the value 1

The zero flag (Z-Flag) is set to 1 if the result of an arithmetic operation is zero.

The control flags are used to control certain modes of the CPU.

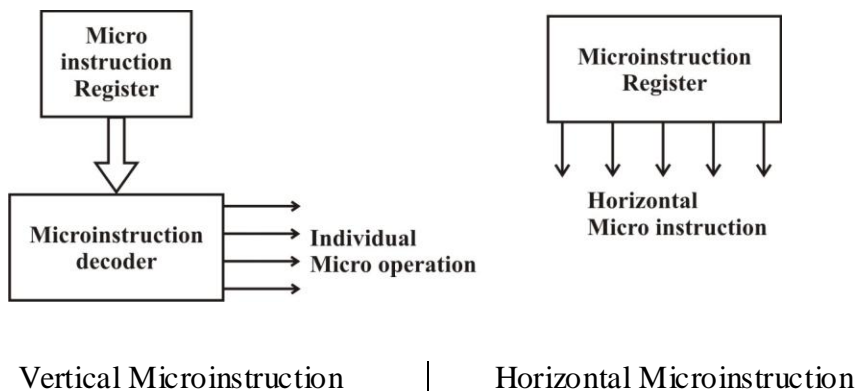


**Sol. 7(a)**



1. Hardwired control is used to generate control signal by use of Finite State Machine while microprogramming is a control mechanism to generate control signals by use of a memory called control storage which contains control signals.
2. Hardwired is hardware design while microprogramming is firmware design
3. Hardwired is faster and microprogramming is slow
4. Hardwired is less complex and less flexible while microprogramming is more flexible and more complex.

**Sol. 7(b)**





- |   |   |
|---|---|
| → More time                                     | → More bits                             |
| → For n-micro operation we need $\log_2 n$ bits | → For n-micro operation, we need n-bits |
| → Considerable encoding                         | → little encoding                       |
| → Limited parallelism                           | → High degree of parallelism            |
| → Short format                                  | → Long format                           |

### Sol. 7(c)

```
#include<stdio.h>
int main(){
    int num,i,count=0;
    printf("Enter a number: ");
    scanf("%d",&num);
    for(i=2;i<=num/2;i++){
        if(num%i==0){
            count++;
            break;
        }
    }
    if(count==0 && num!= 1)
        printf("%d is a prime number",num);
    else
        printf("%d is not a prime number",num);
    return 0;
}
```

Sample output:

```
Enter a number: 5
5 is a prime number
```

### Sol. 7(d)

1. C is Procedural Language but C++ is non Procedural i.e. Object oriented Language.
2. No virtual Functions are present in C The concept of virtual Functions are used in C++.
3. In C Polymorphism is not possible but it is used in C++.
4. Top down approach is used in program Design in C while C++ uses bottom up approach
5. Operator overloading is not present in C but it is present in C++