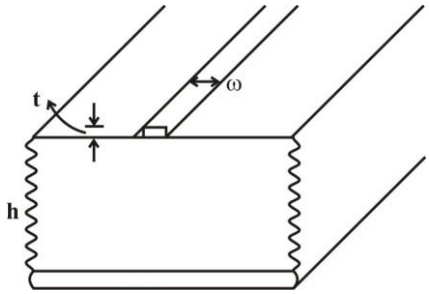
Microwave & Microprocessor Objective Solution

1. (D) Light amplification by stimulated emission of radiation.
MASER (Microwave amplification by stimulated emission of radiation.)

2. (D) In Ruby MASER, mag. Field is provided for frequency adjustment.
Ruby MASER & parametric amplification both are cooled where parametric amplification is cooled to improve noise temperature while Ruby MASER is cooled because it can't operate at room temperature.

3. (C) Micro strip line has Quasi TEM mode i.e. there are only few regions in which there is a component of electric field & mag. in direction of wave propagation.



Since it is open, so there will be radiation loss & there radiation loss be minimized by using a thin dielectric constant having high value. Since energy will be stored in air & in some portion of dielectric constant.

$$\in_{re} = 0.475 \in_r + 0.67$$

$$\boxed{\frac{\in_r + 1}{2} < \in_{re} < \in_r}$$

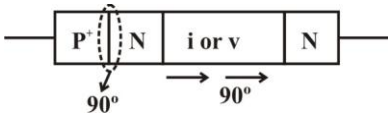
4. (C) Strip line has lower Q factor than waveguide and also has lower power handling capability.

5. (C) $z_0 = \frac{377}{\sqrt{\in_r}}\left(\frac{h}{\omega}\right) = \frac{377}{\sqrt{9}} \times \frac{0.5}{2} = \frac{377 \times 0.5}{6} = 31.4\Omega$

6. (D) $\text{Gain} = \frac{f_o}{f_s}, \quad f_o = f_s + f_p$

7. (C) Parametric amplification uses a variable capacitor or varactor which uses AC source.

8. (B)



BARITT Diode works in forward biased & holes are moving in drift space due to applied voltage & not by avalanche multiplication.

9. (B) During plasma extraction, e′ will have more transit time & current pulse is produced which will (↑) the transit time & power dissipation (↓) so that its efficiency (↑).

10. (B)

11. (C) $\text{Gain} = \left(\frac{R_T + R_L}{R_T - R_L}\right)^2 = \left(\frac{40+80}{40-80}\right)^2 = 9$

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12. (C) For reciprocal $[s]^T = [s]$ & For loss less $[s][s^*] = I$

13. (D) It has high speed & low noise.

14. (A) since TWT has high B.W i.e. why circuit should be non-resonant.

15. (B) TWT is preferred due to its high bandwidth

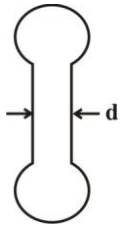
16. (B) Crystal diode, Schottky & Backward are used for detector.

17. (C)

18. (C)

19. (A) Transit time mode has low efficiency because new domain will be formed until all domain reach at anode. $n < 10\%$

20. (D) $\theta_g = \omega \cdot \tau_g = \dfrac{\omega d}{v}$ $d \rightarrow$ cavity distance



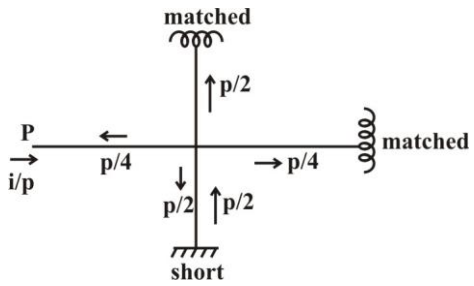
21. (C) Isolator is a two port of device which provides small amount of attenuation from port (1) & (2) and provides more attenuation from (2) to (1). It is used in TWT

22. (A) It is phase difference between two anode cavities

23. (D)

24. (D)

25. (C)



$p_r = p/4$

$p_i = p$

$\therefore \quad |k| = 1/2 = 0.5$

$\therefore \quad \boxed{VSWR = 3}$

26. (C)

27. (B)

28. (D)

29. (B)

30. (C)

31. (B)

32. (A)

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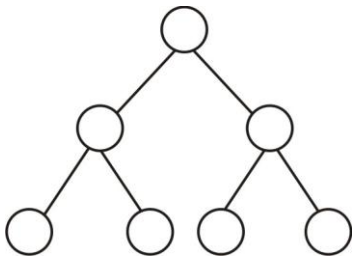
33. (A)
34. (A)
35. (A)



No. of nodes = 7

Depth $= \log_2(n+1) - 1 = 3 - 1 = 2$

Leaf nodes $= 4 = 2^2$

36. (B)
37. (D) Total Number of spanning tress equal to n^{n-2}
38. (A) Depth of graph is $\log_2(n+1) - 1$
39. (B)
40. (B)
41. (D)
42. (C) Cache memory time $= (24 - 45)\,n\,sec$
43. (A) Average access time $= Avg \cdot seek + Avg.\,Latency\,time + Time\,in\,Transfer\,rate$

Avg. Latency time $= \frac{0.5}{RPS} = \frac{0.5}{30} = \frac{1}{60} \approx 16.67\,m\,sec$

$\therefore$ Avg. access time $= 30 + 16.67 \approx 47\,m\,sec.$

44. (A) 8.196 m sec Avg. Latency time $= \frac{0.5}{3660} \times 60 = 8.196\,m\,sec$
45. (B)
46. (A) Register has the fastest memory
47. (A) 1st cycle is Fetch cycle
48. (D)
49. (A)
50. (B) Translate mode $\rightarrow$ cycle steal mode
51. (D)
52. (A) RISC $\rightarrow$ Fix length
    Single wire
    Hard wire
    Register to Register
    Few instructions & few addressing mode.
53. (A)
54. (A)

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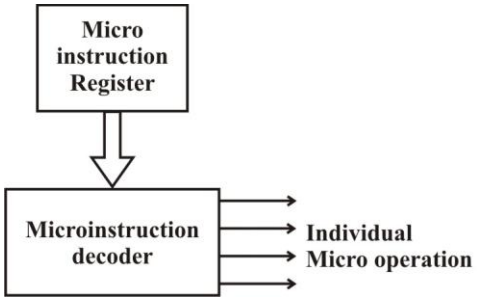

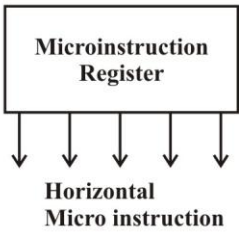

Vertical Microinstruction	Horizontal Microinstruction
→ More time	→ More bits
→ For n-micro operation we need $\log_2 n$ bits	→ For n-micro operation, we need n-bits
→ Considerable encoding	→ little encoding
→ Limited parallelism	→ High degree of parallelism
→ Short format	→ Long format

55. (B) $T_S = T_C \times H + T_M \times (1-H)$

$T_C \rightarrow$ Cache memory

$T_M \rightarrow$ For main memory

$T_S = 0.95 \times 10 + 100 \times 0.05 = 9.5 + 5$

$T_S = 14.5\,\text{n sec}$

56. (B)

57. (D) $\dfrac{\lfloor 2n}{\lfloor n \lfloor n+1} = 5$

58. (B)

59. (C)

60. (C)

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