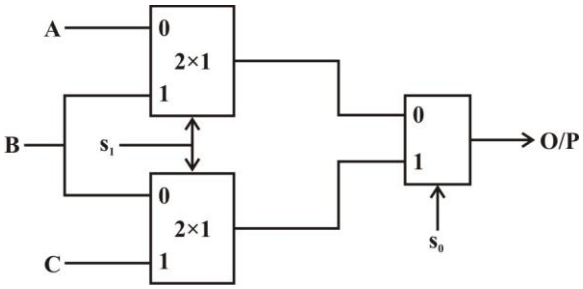
DIGITAL Conventional Solution (ESE-2015 Test Series Dated 08.05.2015)

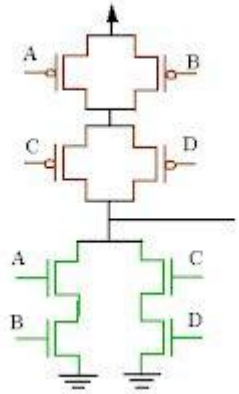
Sol.1 (a) MOD-60 counter is used to divide time by 60.

Sol.1 (b)



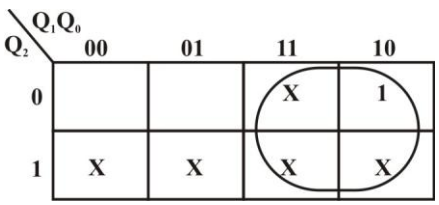
Sol.1 (c) $P - D_{in}$ $Q - s_2$ $R - s_0$ $S - s_1$

Sol.1 (d) CMOS as EX-OR gate:

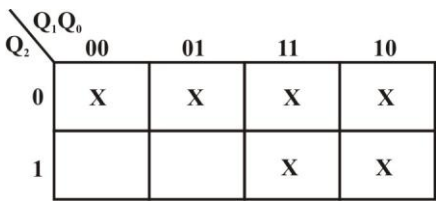


Sol.2(a)

Q_2	Q_1	Q_0	J_2	k_2	J_1	k_1	J_0	k_0
0	0	0	0	x	0	x	1	x
0	0	1	0	x	1	x	x	1
0	1	0	1	x	x	1	0	x
1	0	0	x	0	0	x	1	x
1	0	1	x	0	1	x	x	1
1	1	0	x	1	x	1	0	x



$J_2 = Q_1$



$k_2 = \bar{Q}_2$

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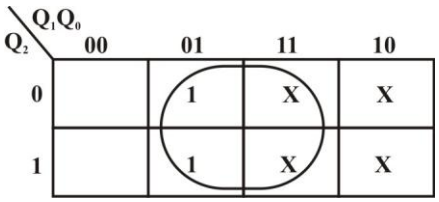
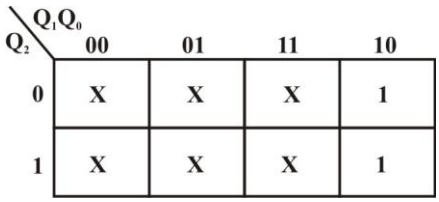
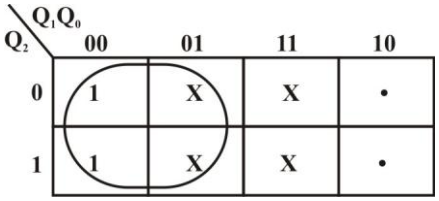


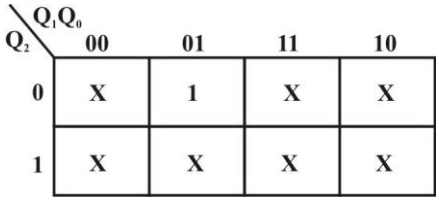
$J_1 = Q_0$



$k_1 = 1$



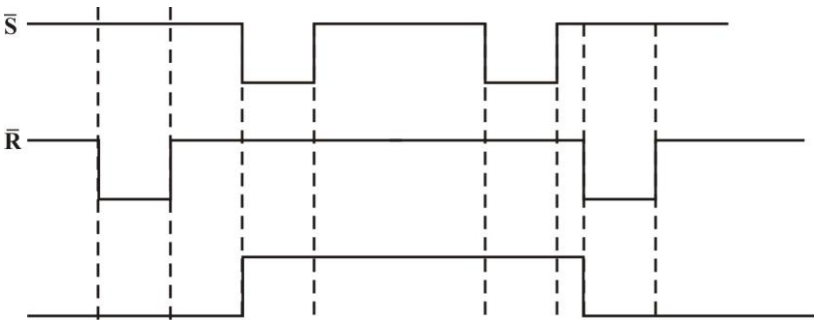
$J_0 = \overline{Q}_1$



$k_0 = 1$

Sol. 2(b) This is standard R-S FF or Latch

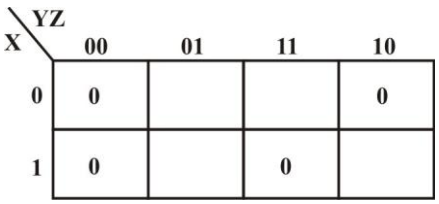
R	S	Q_{n+1}	$\overline{R}$	$\overline{S}$	Q_{n+1}
0	0	Q_n	1	1	Q_n
0	1	1	1	0	1
1	0	0	0	1	0
1	1	??	0	0	??



Sol.3(a)

E	Data – In	X(address)	Q_{n+1}	Data Out
0	X	X	0	0
1	0	X	0	0
1	1	1	1	1
1	1	0	0	0

Sol.3(c)



$F = (X+Z)(X+Y+Z)(Y+Z)$

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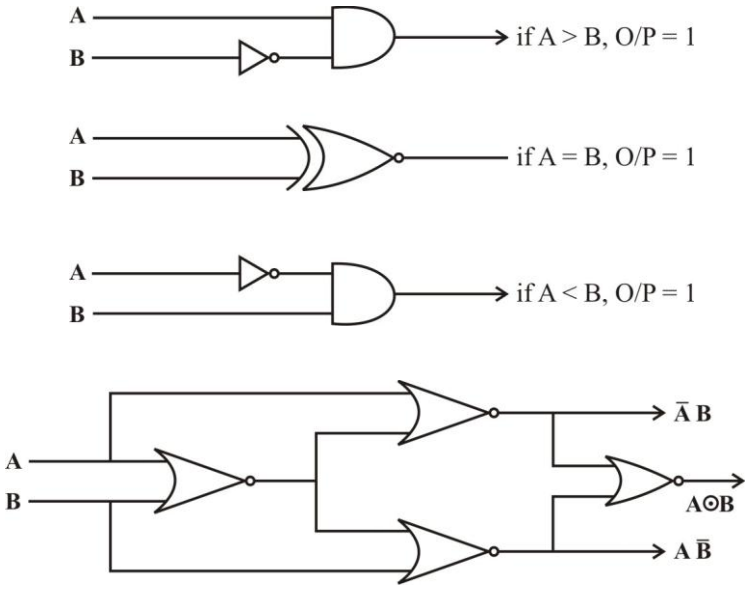
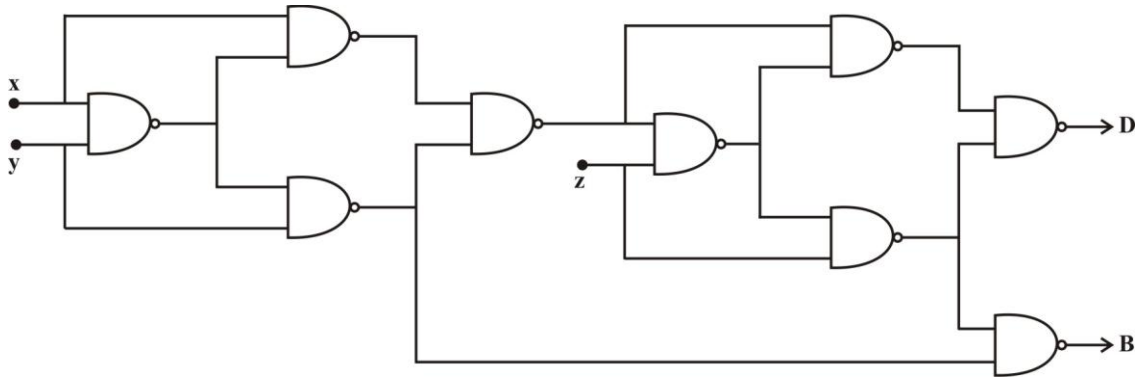
Sol.4 (a)



Sol.4 (b) Full subtractor is designed by use of 9 gates.



Sol.4(c)

Q_2	Q_1	Q_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	$\overline{P_r}$	$\overline{Cl_r}$	$\bar{Q}(up)$	$Q(Down)$
0	0	0	1	1	1	1	1	1	1	0	1	0	1	0
0	0	1	1	1	1	1	1	1	0	1	1	1	1	0
0	1	0	1	1	1	1	1	0	1	1	1	1	1	0
:				:						:		:		:
1	0	1	1	1	0	1	1	1	1	1	0	1	0	1

Down counter starts row. Sequence: 0, 1, 2, 3, 4, 5, 4, 3, 2, 1, 0, 1, 2, 3.

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Sol.5 (a) Quantization error $= \frac{1}{2^N - 1}$ where N = 12

$$\text{Error} = \frac{1}{2^{12} - 1} = 0.025\%$$

Sol.5 (b) $2V \rightarrow +127 \qquad -2V \rightarrow -128$

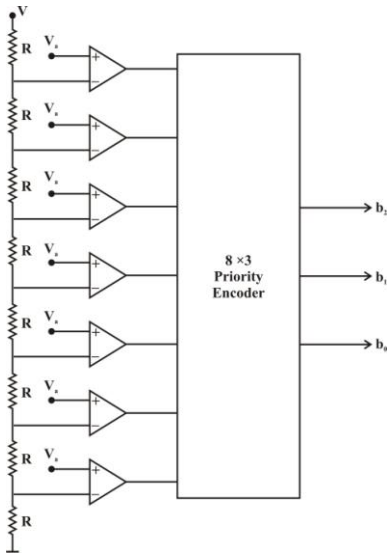
$$-1.5 \rightarrow \frac{-128}{2} \times 1.5 = -96$$

$$96 \rightarrow 01100000$$
$$\downarrow$$
$$10011111$$
$$+ \quad 1$$
$$\overline{10100000}$$
$$\Downarrow$$
$$A0H$$

Sol.5 (c) Range will be: (2000 – 3FFF)

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	$A_{10} - - - -$	A_0
0	0	1	0	0	0 – – – –	0
0	0	1	1	1	1 – – – –	1

Sol.5 (d)



Sol.6 (a)

Logic Family	Propg.delay(ns)	Power dissipation (mW)	Fan-in	Fan-out	Noise margin
RTL	12-30	15	4	4	0.2-0.4
DTL	30	12	10	8	0.7
TTL	5-15	10	8	10	0.4
ECL	2-4	50	5	16-20	0.4
I^2L	1	0.1	5	8	0.35
PMOS	50	1	8	20	0.4
CMOS	70	0.01	8	50	5

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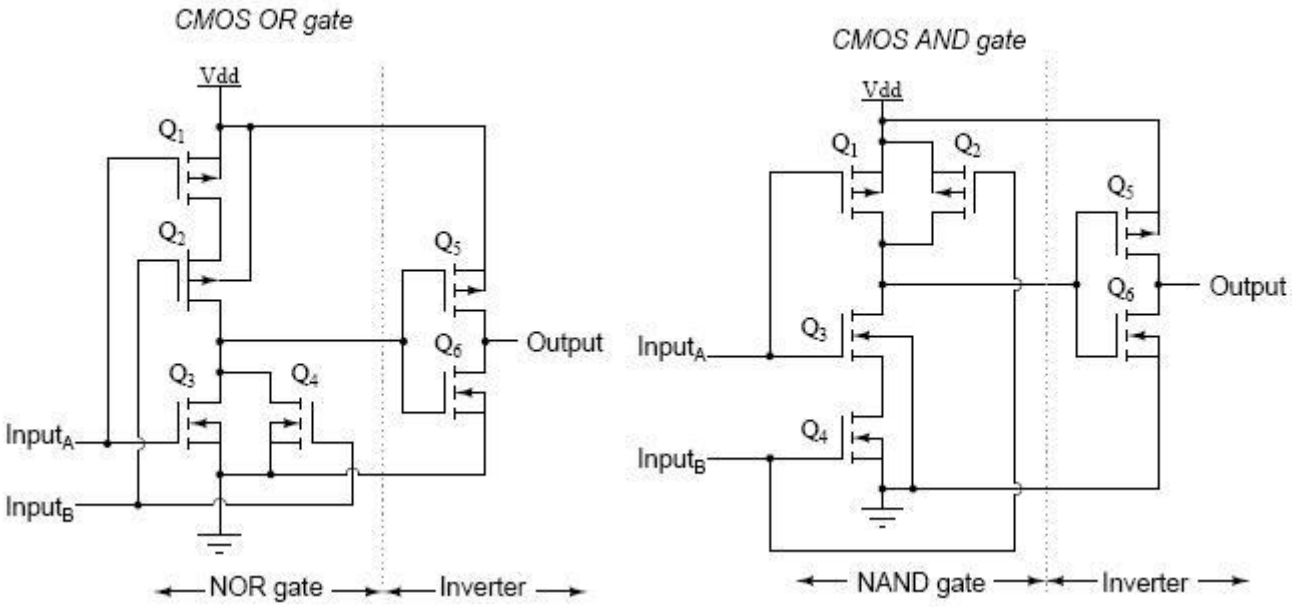
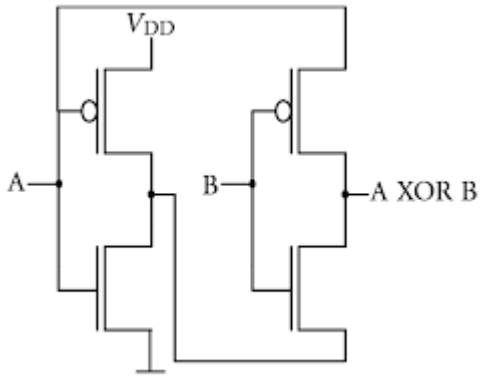
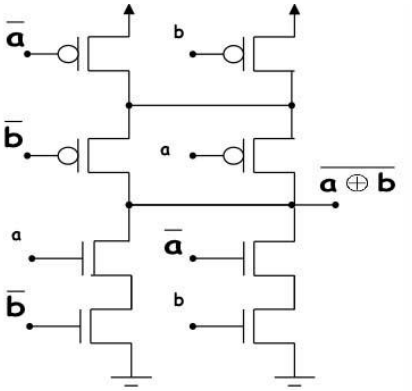
Sol.6 (b)







Sol.6 (c)

Case-1: when control input is Low:

When one of the input of emitter of Q_1 is LOW whatever may be data input Q_3 and Q_2 to turn off Here both Q_3 and Q_4 in totem pole are off and output of circuit behaves like an open circuit with a very high output impedance.

Case-2: when control input is High:

(i) when data input is Low: Output is high

(ii) when data input is High: Output is low

Sol.7 (a) $Q_n = 1$ $B = 0$

Initially Q_n=0=A=B

After 1 clock cycle output of FF will be 1 and counter will be enable and A=0 and B=1

After 2 clock cycle output of FF will be 0 and counter will be disable and A=0 and B=1

After 3 clock cycle output of FF will be 0 and counter will be disable and A=1 and B=0

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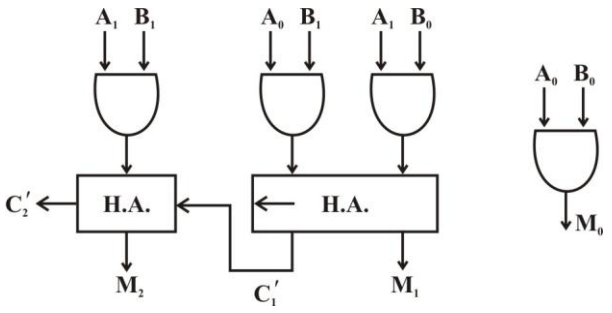
Sol.7 (b) Here Y=X+1 and if base is r then rX+Y=25 and rY+X=31

By solving all 3 equations

Base(r) = 7 X = 3 Y = 4

Sol.7 (c) $(5000-57FF)H$

Sol. 7(d)



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