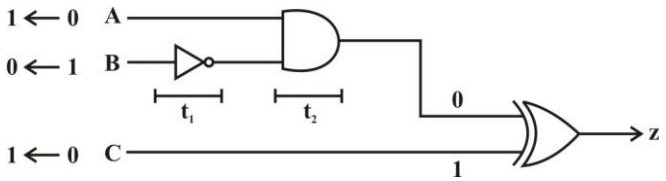
Digital Objective Solution

1. (C)
2. (C)
3. (A) $00001000 \rightarrow +8$
   $10001000 \rightarrow -8$
4. (D) Shift register changes spatial code to temporal code
5. (A) Solve By K-MAP Method
6. (C)
   V_{OH}(min)=2.4 Volt V_{OL}(max)=0.4 Volt
   V_{IH}(min)= 2.0 Volt V_{IL}(max)=0.8 Volt
7. (B)
8. (D)
9. (D) Number of bits for 64 Alphanumeric are $35 \times 64 = 2240$
10. (D)
11. (C) Overflow means if 2 +ve no. are added and result is –ve.
    if 2 –ve no. are added and result is +ve.
12. (D) In 1's complement operation, carry will be added again which will make hardware complex.
    In 2's complement, no need to add carry again.
13. (A) $1000 \rightarrow -8$
    2's 0111
    $\underline{+\ 1}$
    1000

No chance of over flow if one number is positive and other is negative

14. (C)
15. (B) XS=64 =64+Number
16. (D)
17. (B)
18. (C) There are three states HIGH LOW and HIGH Impedance state
19. (C) DECODER followed by OR gate where OR is programmable
20. (C) D-latch is designed by S-R flip-flop which is used for binary storage.
21. (A)
22. (D)
23. (A)
24. (B)



After $t_1 + t_2 \rightarrow$ z will become 0.

$\therefore \quad 20 + 20 = 40\,\text{n sec}$

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After $40\,\text{n sec}$; $z = 0$

$\therefore$ z will remain for 40 n sec.

25. (A) If n is no of variables in k-map.

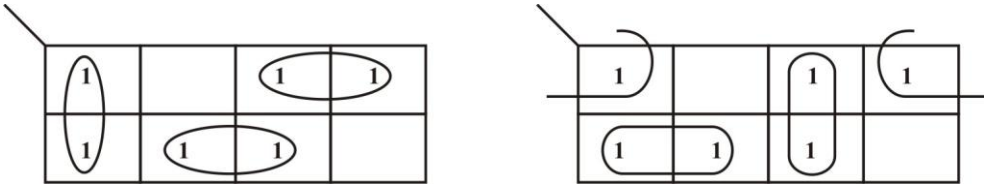
2^m are no. of 1's and 0's in pair.

No. of variables = $(n-m)$

$n = 9 \qquad 2^m = 64 = 6$

$(n-m) =$ No. of literals = 3.

26. (A)



No '1' is not loyal to a single group.

$\therefore$ No. of essential prime implicants = 0

27. (C)

A	B	O/P
0	0	0
0	1	1
1	0	1
1	1	0

If light is already ON, then by making ON either of the switch, light will become off.

28. (B) XOR gate is not universal gate

29. (B)

30. (A) OR gate does not means addition irrespective of inputs.

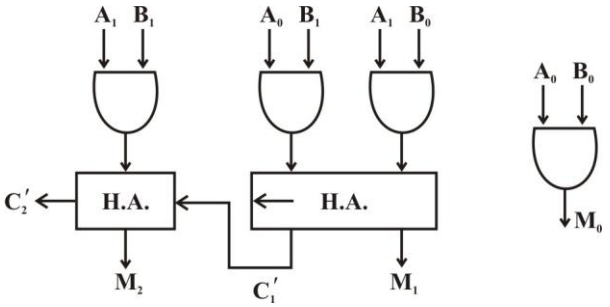
31. (C)

32. (B) For n variables maximum number of prime impilcants are 2^{n-1}

33. (B) $f(A,B,C) = A \oplus B \oplus C = \sum(1,2,4,7)$

34. (A)

35. (B)



36. (D) K-Map minimizes number of literals and number of terms in expression

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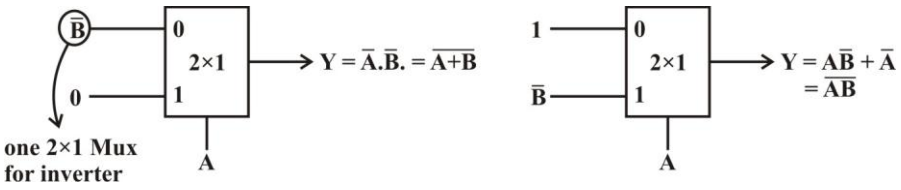
37. (D)



38. (C) It remains between cut-off and active region.

39. (A) It uses both NPN and PNP transistor

40. (C)

41. (A) CMOS has highest value of fan-out due to high value of input impedance.

42. (C) Tri state have high impedance not switching speed

43. (D)

44. (D) $5\left(\frac{1}{200}+\frac{1}{100}+\frac{1}{25}\right)=\frac{0-V_{out}}{10}$

$V_{out}=-(2+0.5+0.25)=-2.75$

45. (D)

46. (B)

A_1	A_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	1	0	0
1	1	1	0	0	1

Simply grounded Coming directly from A_0

47. (B)

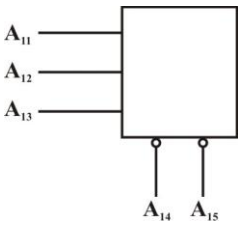
48. (A) $V_0=\frac{V_R}{2^n}=\frac{4\times 2}{8}=1$

49. (D) PROM $\rightarrow$ Fixed AND + Programmable OR.

PAL $\rightarrow$ Programmable AND + Fixed OR

PLA $\rightarrow$ Both AND and OR programmable

50. (C)



11 address lines left for memory blocks.

$\therefore$ Memory $\rightarrow 2^{11}=2k$ Bytes = 16 k bits

51. (B)

52. (D) Mod -2 counter

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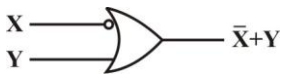
53. (A)

54. (D)

55. (C)

56. (C)



Universal gate $= \overline{AB} = \bar{A} + \bar{B}$

$A = X, \quad B = \bar{Y}$

57. (B)

58. (D)

59. (C)

60. (B)

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